DATA SHEET

TDA9170
YUV picture improvement processor based on histogram modification

Preliminary specification
File under Integrated Circuits, IC02

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Philips Semiconductors

PHILIPS

YUV picture improvement processor based on histogram modification

TDA9170

FEATURES

- Picture content dependent non-linear Y and U, V processing by histogram analysis
- Adaptive and variable gamma correction controls
- Black and white stretch capabilities
- Transparent I²C-bus control
- On-chip window generator for valid histogram measurement and black detection.

GENERAL DESCRIPTION

The TDA9170 is a transparent analog video processor with a YUV interface. It offers three main luminance processing functions any combination of which can be selected.

The luminance transfer is controlled in a non-linear manner by the distribution (in 5 discrete histogram sections) of the luminance values measured in a picture. As a result, the contrast ratio of the most important parts of the picture will be improved.

Black restoration is available in the event of a set-up in the luminance signal. A variable gamma function, after the histogram conversion, offers the possibility of excellent brightness control.

To maintain a proper colour reproduction, the saturation of the U and V colour difference signals are controlled as a function of the actual non-linearity in the luminance channel.

The TDA9170 concept has maximum flexibility with the optional on-board I²C-bus (including hardwired address select) and window control. The supply voltage is 8 V. The device is mounted in a 32 pin SDIP envelope.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9170	SDIP32	plastic shrink in-line package; 32 leads (400 mil)	SOT232-1

BLOCK DIAGRAM

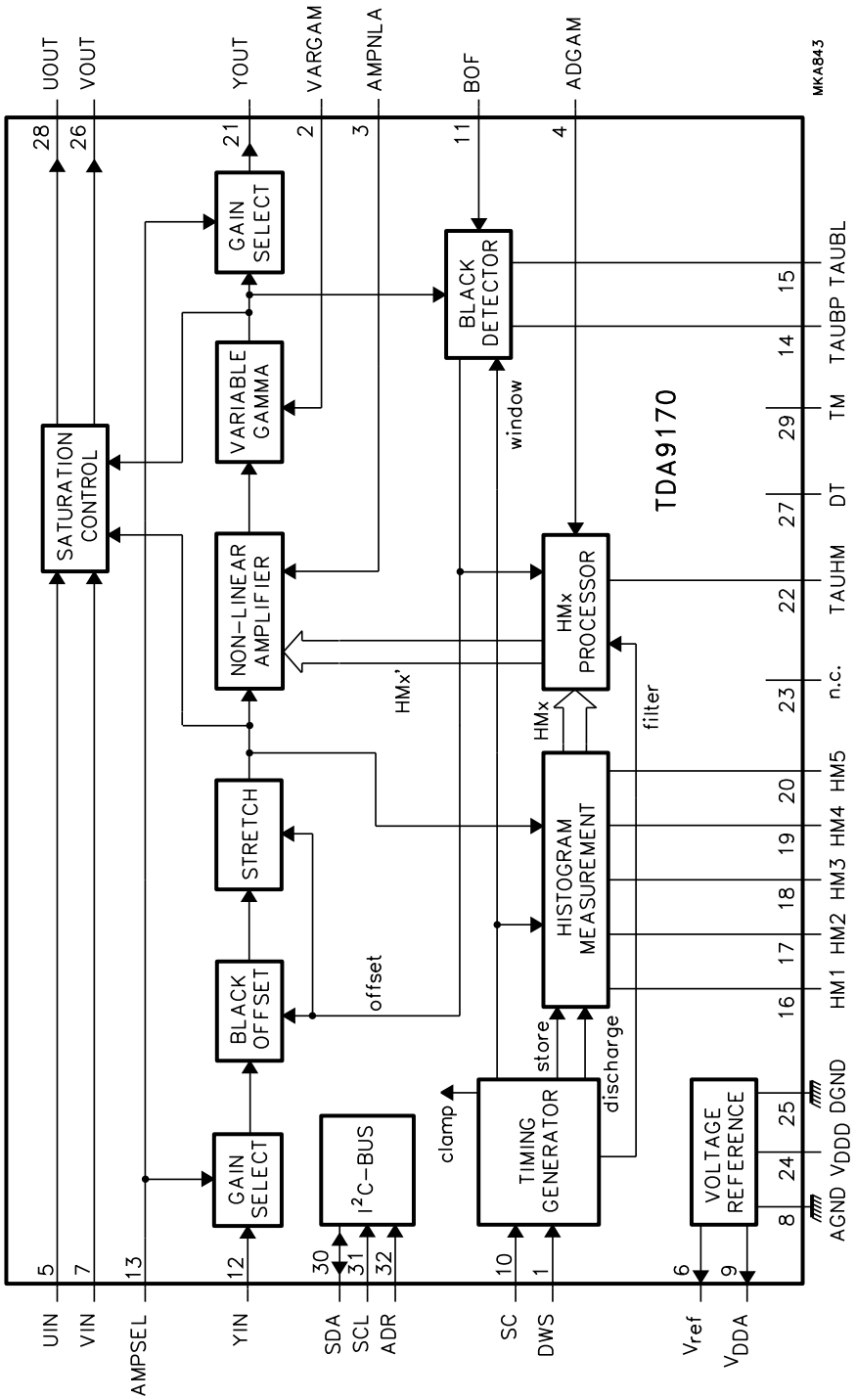


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
DWS	1	default window select input
VARGAM	2	variable gamma input
AMPNLA	3	amplitude non-linearity input
ADGAM	4	adaptive gamma input
UIN	5	colour difference U input
V_{ref}	6	reference supply voltage output (+4 V)
VIN	7	colour difference V input
AGND	8	analog ground
V_{DDA}	9	analog supply voltage
SC	10	sandcastle input
BOF	11	black offset on/off input
YIN	12	luminance input
AMPSEL	13	amplitude select input
TAUBP	14	time constant black peak
TAUBL	15	time constant black loop
HM1	16	histogram segment memory 1
HM2	17	histogram segment memory 2
HM3	18	histogram segment memory 3
HM4	19	histogram segment memory 4
HM5	20	histogram segment memory 5
YOUT	21	luminance output
TAUHM	22	time constant histogram measurement loop
n.c.	23	not connected
V_{DDD}	24	digital supply voltage (+5 V)
DGND	25	digital ground
VOUT	26	colour difference V output
DT	27	test option
UOUT	28	colour difference U output
TM	29	test option
SDA	30	serial data input/output (I^2C-bus)
SCL	31	serial clock input (I^2C-bus)
ADR	32	address select input (I^2C-bus)

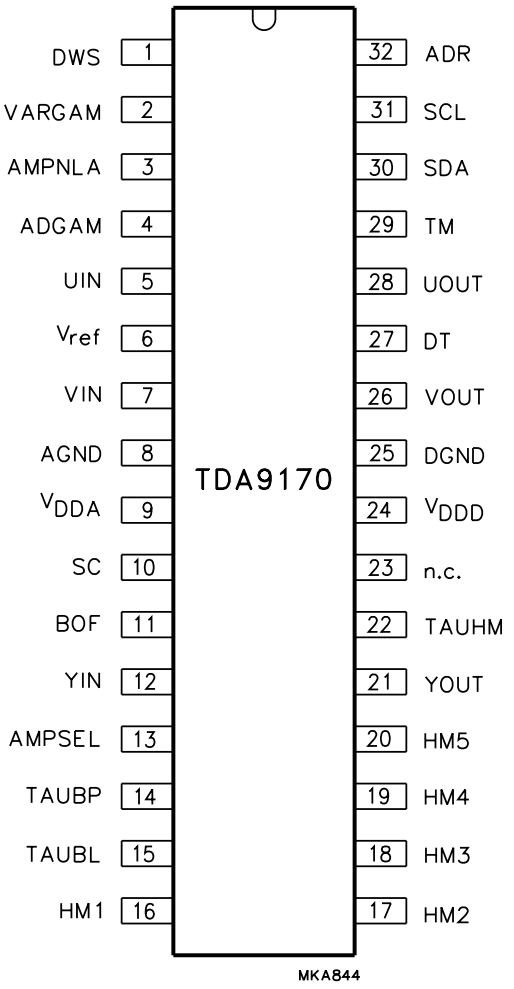


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Y input selection and amplification

The dynamic range of the luminance input amplifier can be switched between 0.3 and 1 V (excluding sync) either externally (pin AMPSEL) or by I²C-bus (AMPSEL bit). Amplitudes that exceed the corresponding specified range (e.g. the sync) will be clipped internally. The input is clamped during the logic HIGH period of the clamp which is defined by the sandcastle reference and should be DC-decoupled with an external capacitor.

Black offset detection and correction

The black detector measures and stores the blackest part of the picture within a defined window in each field. Any difference between this value and the value measured during the black clamp period is regarded as black offset. In a closed loop configuration, the black offset is held until a predefined value of the full scale (FS) value is fed back to the input stage where it is partly compensated for. Depending on the loop gain, 30% to 50% of the offset value is counteracted. The loop gain is also a function of the adaptive and variable gamma settings. The black offset correction mechanism can be switched on and off by the I²C-bus via the BON bit (see Table 6), or externally with the black offset on/off switch (BOF pin 11).

Two external time constants are required to ensure correct performance of the black detector; a loop filter time constant (TAUBL) for the loop dynamics and a time constant for memorizing the darkest parts of the picture (TAUBP) in just one field. During the field retrace the time constant TAUBP is first sampled and then preset to a value that corresponds to the maximum black offset.

The corrected black offset is related to the nominal signal amplitude which is reset to 100% FS via an amplitude stretch function. Luminance values beyond FS are not affected. Additionally, this offset is also used to set the adaptive gain (see Section “Adaptive gamma”).

Histogram measurement

The histogram distribution is measured in real time over five segments (HM1 to HM5) within a defined window period of each field. During the window period, the video is in one segment, a corresponding external capacitor C_{HMx} is loaded via a current source. At the end of the field five segment voltages are stored from the external capacitors into on-board memories. The external capacitors are discharged and the measurements are restarted.

Any part of the picture that does not contribute to the information within the total picture should be omitted from the histogram measurement. The miscount detector disables measurements until it detects changing parts. Additionally, luminance values close to FS (or white) do not contribute sufficiently in order to maintain the absolute light output. This procedure is allowed because the eye is less sensitive to details in white.

As the miscount detector shortens the effective measurement period and, because of spreads of internal and external components, the current source is controlled within in a closed loop so as to maintain a constant average value of the sum of the segment voltages. The dominant time constant of the closed loop is external and can be tuned with an appropriate capacitor connected to TAUHM (pin 22).

Processing of the measured histogram values

Field averaging of histogram values

With very rapid picture changes, also related to the field interlace, flicker might result. The histogram values are averaged at the field rate to reduce these flicker effects. The time constant of the averaging process is adapted to the speed of the histogram changes.

Adaptive gamma

The output voltage of the first segment is fed to a variable gain amplifier with a gain between 1 and 3. In this way luminance values in the ‘black’ segment have a larger weight. In our perception black parts are expanded, as occurs with gamma control. However, the effective contribution to the non-linear gain is only relevant for moderate segment voltages and hence the term adaptive gamma.

The adaptive gamma gain is a **max**-function of a fixed gain part and a dynamic gain part. The fixed gain part can be set externally with the adaptive gamma gain control (ADGAM) or via the I²C-bus.

The dynamic part of the adaptive gamma gain is controlled by the measured black offset value from the black detector.

ADAPTIVE WHITE-POINT STRETCHING

For dominant HM4 and HM5 voltages or large white parts the histogram conversion procedure makes a transfer with large gain in the white parts. However, the amount of light being emitted from the picture is considerably reduced. The white stretcher introduces additional overall gain for increased light production and, as a result, violates the principle of having a full-scale reference.

STANDARD DEVIATION

For pictures in which segments of the histogram distribution are very dominant, with respect to the others, the non-linear amplification should be reduced to compensate for pictures with a flat histogram distribution. The standard deviation detector measures the spread of the histogram distribution in the segments HM1 to HM5 and modulates the user setting of the non-linear amplifier.

Non-linear amplifier

The stored segment voltages, relative to their average value and averaged over two fields, determine the individual gain of each segment in such a way that continuity is guaranteed for the complete range. The maximum and minimum gain of each segment is limited. Apart from the adaptive white-point stretching the black and white references are not affected by the non-linear processing. The amount of linearity can be controlled externally at AMPNLA (pin 3) or via the I^{2}C-bus.

Variable gamma function

As well as the histogram conversion, a variable gamma function can be applied to ensure excellent brightness control. It is intended as an alternative to the DC-offset of the classic brightness user control; it maintains the black and white references. The gamma ranges from 0.5 to 1.5. The gamma can be set externally at VARGAM (pin 2) or via the I^{2}C-bus.

Colour compensation

Non-linear luminance processing influences the colour reproduction, mainly the colour saturation. Therefore, U and V signals are also processed for saturation compensation. The U and V input signals are clamped during the logic HIGH period of the clamp which is defined by the sandcastle reference and should be DC decoupled with external capacitors.

Timing generator

The TDA9170 is equipped with a transparent internal timing generator for window purposes. As a timing reference the relevant sandcastle (SC) can be used. The window enables the black measurement and the histogram measurement circuitry. The internal timing generator is basically intended for system invariant operation. The default window handles all existing norms and disables measurement in subtitles or logos. This default window is preset at power-up and can be selected with a logic HIGH level at the default window select DWS (pin 1). If not selected the blanking of the sandcastle will define the window borders.

However, using the I^{2}C-bus and setting the WD1 and WD2 control bits (see Table 3), the window format can also be user-programmed. The horizontal window generator synchronizes on the rising edge of the burst key/clamp key of the external sandcastle reference with an adjustable window start and stop delay. The vertical window generator synchronizes on the falling edge of the first burst key/clamp key after a field pulse recognition.

I^{2}C-bus specification

The I^{2}C-bus is designed for transparent use. At power-up all registers are preset for system invariant and external control. All pins related to the I^{2}C-bus can be left open-circuit when the I^{2}C-bus is in the standby mode. If the sleep mode bit in the control register is set all settings are left to bus control. For the relevant registers and addresses see Tables 2 to 8.

Table 1 Slave address.

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	0	ADR	X

Table 2 Control function.

CONTROL FUNCTION	TYPE	SUB-ADDRESS(1)	DATA BYTE							
			D7	D6	D5	D4	D3	D2	D1	D0
Control	REG	00	X	X	X	BON	WD2	WD1	AMS	SLP
User variable gamma	DAC	01	X	X	D5	D4	D3	D2	D1	D0
Adaptive gamma	DAC	02	X	X	D5	D4	D3	D2	D1	D0
Non-linear amplifier	DAC	03	X	X	D5	D4	D3	D2	D1	D0
Line start stop	REG	04	ST3	ST2	ST1	ST0	SP3	SP2	SP1	SP0
Field start stop	REG	05	ST3	ST2	ST1	ST0	SP3	SP2	SP1	SP0
Status	REG	–	X	X	X	X	X	X	X	POR

Note

1. Valid sub-addresses: 00 to 05 (HEX); auto-increment mode available for sub-addresses.

Table 3 Window select bits (WD1 and WD2).

WD1	WD2	FUNCTION
0	0	default window
0	1	window by sandcastle blanking
1	X	user window

Table 4 Amplitude select bit (AMS).

LOGIC LEVEL	FUNCTION
0	0.3 V luminance
1	1 V luminance

Table 5 Sleep mode bit (SLP).

LOGIC LEVEL	FUNCTION
0	sleep
1	I^2C-bus control

Table 6 Black offset compensation enable bit (BON).

LOGIC LEVEL	FUNCTION
0	disabled
1	enabled

Window formats

Table 7 Line frequency start stop format.

LINE WINDOW(1)	TIMING(2)	UNIT
Start (LWS)	$^{4.5}/_{64fh} + {}^{1}/_{64fh} \times$ DEC(ST3, ST2, ST1, ST0)	µs
Stop (LWP)	$^{26.5}/_{64fh} + {}^{2}/_{64fh} \times$ DEC(SP3, SP2, SP1, SP0)	µs
Default	DEC(ST3, ST2, ST1, ST0) = 2 DEC(SP3, SP2, SP1, SP0) = 14	

Notes

1. Start and stop events are relative to the leading edge of the BK/CLP pulse of the sandcastle.
2. fh is defined as the line frequency.

Table 8 Field frequency start stop format.

FIELD WINDOW(1)	TIMING	UNIT
Start (FWS)	10 + 6 × DEC(ST3, ST2, ST1, ST0)	lines
Stop (FWP)	121 + 10 × DEC(SP3, SP2, SP1, SP0)	lines
Default	DEC(ST3, ST2, ST1, ST0) = 9 DEC(SP3, SP2, SP1, SP0) = 4	

Note

1. The start event is relative to the trailing edge of the first BK/CLP pulse after a field pulse recognition. The stop event is relative to the actual start event.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage		–0.5	+8.8	V
V_{DDD}	digital supply voltage		–0.5	+5.5	V
V_{ref}	reference supply voltage		–0.5	+5.5	V
V_n	voltage input/output on any other pin		–0.5	V_{DDA} + 0.5	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–10	+70	°C
V_{es}	electrostatic discharge	note 1	–2000	+2000	V
		note 2	–200	+200	V

Notes

1. Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
2. Machine model: equivalent to discharging a 200 pF capacitor through a 0 Ω resistor.

QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611 part E"*. The numbers of the quality specification can be found in the *"Quality Reference Handbook"*. The Handbook can be ordered using the code 9398 510 63011. All pins are protected against electrostatic discharge by means of clamping diodes.

Latch-up

At T_{amb} = 70 °C all pins meet the specification as follows, except for pins 6 and 7 at positive trigger currents:

$I_{trigger} > 100$ mA or $V_{pin} > 1.5V_{DDA(max)}$.

$I_{trigger} < -100$ mA or $V_{pin} < -0.5V_{DDA(max)}$.

pin 6, V_{ref}: $I_{trigger} > 40$ mA or $V_{pin} > 1.5V_{DDA(max)}$.

pin 24, V_{DDD}: $I_{trigger} > 70$ mA or $V_{pin} > 1.5V_{DDA(max)}$.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	48	K/W

CHARACTERISTICS

V_{DDA} = 8 V; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pins 6, 9 and 24)						
V_{DDA}	analog supply voltage		7.2	–	8.8	V
V_{DDD}	digital supply voltage		–	5.0	–	V
V_{ref}	reference supply voltage		–	4.0	–	V
I_{DDA}	analog supply current		–	40	–	mA
$Z_{o(24)}$	output impedance		–	–	250	Ω
$Z_{o(6)}$	output impedance		–	–	250	Ω
Luminance input/output selection						
LUMINANCE INPUT (PIN 12); note 1						
$V_{i(Y)}$	luminance input voltage	AMPSEL = 0	0.3	–	–	V
		AMPSEL = 1	1.0	–	–	V
$V_{i(Yclamp)}$	input voltage level during clamping		–	1.5	–	V
$I_{ib(Y)}$	input bias current		–	–	0.1	µA
LUMINANCE INPUT VOLTAGE RANGE SELECTION AMPSEL (PIN 13); note 2						
$V_{i(SEL)l}$	input voltage selection for lower range		–	–	1.5	V
$V_{i(SEL)h}$	input voltage selection for higher range		3.5	–	–	V
$I_{ib(SEL)}$	input bias current		–	–	0.1	µA
LUMINANCE OUTPUT (PIN 21)						
$V_{o(Y)}$	luminance output voltage	AMPSEL = 0	0.3	–	–	V
		AMPSEL = 1	1.0	–	–	V
$V_{oYclamp}$	output voltage level during clamping	AMPSEL = 0	–	2.9	–	V
		AMPSEL = 1	–	2.0	–	V
V_{no}	output noise voltage		52	–	–	dB
B_Y	luminance bandwidth	transparent	7	9	–	MHz
$B_{Y(nl)}$	non-linear processing luminance bandwidth		10	–	–	MHz
E_{bl}	black level error	no offset; transparent	–	–	1	%
$E_{G(n)}$	nominal gain error	no offset; transparent	–	–	8	%
Black detection and correction						
BLACK DETECTOR						
$BI_{osd(max)}$	maximum black offset detection at the input		23	25	27	%
$BI_{osc(max)}$	maximum black offset correction at the input		8	10	12	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PICTURE AMPLITUDE STRETCH						
$E_{G(s)}$	gain error after stretch	maximum offset	–	–	1	%
BLACK OFFSET CORRECTION ON/OFF SWITCH BOF (PIN 11); note 2						
$V_{i(blos)}$	input voltage level	correction off	–	–	1.5	V
		correction on	3.5	–	–	V
$I_{ib(blos)}$	input bias current		–	–	0.1	µA
TIME CONSTANT CONTROL TAUBP (PIN 4); see Fig.3						
$I_{BP(d)}$	discharge current		–	–	3.5	mA
I_{ibBP}	input bias current		–	–	0.1	µA
$V_{BP(l)}$	control voltage lower limit		–	1.0	–	V
$V_{BP(h)}$	control voltage upper limit		–	2.5	–	V
TIME CONSTANT CONTROL TAUBL (PIN 5); see Fig.4						
I_{ibBL}	input bias current		–	–	0.1	µA
$V_{BL(l)}$	control voltage lower limit		–	2.0	–	V
$V_{BL(h)}$	control voltage upper limit		–	3.5	–	V
Histogram measurement						
HISTOGRAM UPDATES AT HMx (PINS 16 TO 20)						
Q_{HMb}	segment bleeder accuracy		–	–	2	%
$V_{HM(av)}$	average voltage level for 5 segments		–	1.0	–	V
$V_{HM(min)}$	minimum segment voltage level		0	–	–	V
$V_{HM(max)}$	maximum segment voltage level		–	5.0	–	V
I_{ibHM}	input bias current		–	–	0.1	µA
TIME CONSTANT CONTROL TAUHM (PIN 22); see Figs 5, 6 and 7						
I_{ibTHM}	input bias current		–	–	0.1	µA
$V_{THM(l)}$	control voltage lower limit		–	1.0	–	V
$V_{THM(h)}$	control voltage upper limit		–	2.0	–	V
MISCOUNT DETECTION						
$Q_{mc(d)}$	miscount detection level		–	5	–	%
$t_{p(mc)}$	miscount propagation delay	20% step	–	25	–	ns
$t_{o(mc)}$	miscount detection on-time for each event		0.31	0.36	0.41	µs
$t_{Y(mc)}$	mismatch propagation and luminance delay		–	–	20	ns
$Q_{mc(aW)}$	miscount activation level at white	no miscount	–	90	–	%
$Q_{mc(dW)}$	miscount de-activation level at white	miscount	–	87	–	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Processing of measured histogram values						
ADAPTIVE GAMMA CONTROL RANGE						
$G_{adg(min)}$	minimum gain for HM1		–	1	–	
$G_{adg(max)}$	maximum gain for HM1		–	3	–	
ADAPTIVE GAMMA SETTING ADGAM (PIN 4); note 3; see Fig.8						
$V_{adg(l)}$	control voltage lower limit		–	1.75	–	V
$V_{adg(h)}$	control voltage upper limit		–	3.25	–	V
I_{ibADG}	input bias current		–	–	0.1	µA
$G_{adp(min)}$	minimum gain for HM1	no offset; G_{VAR} = 1	–	1	–	
$G_{adp(max)}$	maximum gain for HM1	no offset; G_{VAR} = 1	–	3	–	
ADAPTIVE GAMMA BY BLACK OFFSET						
$G_{adb(min)}$	minimum gain for HM1	no offset; G_{VAR} = 1	–	1	–	
$G_{adb(max)}$	maximum gain for HM1	maximum offset; G_{VAR} = 1	–	2.5	–	
WHITE-POINT STRETCH						
G_{wp}	maximum gain luminance for white stretch	HM-pattern = 01103: G_{nl} = 1	–	1.09	–	
Non-linear amplifier						
NON-LINEAR GAIN SET BY HMx (PINS 16 TO 20)						
$Q_{nl(b)}$	segment bleeder accuracy		–	–	2	%
$G_{nl(min)}$	minimum gain segment	HM-pattern = 31100: G_{nl} = 1	–	0.36	–	
$G_{nl(max)}$	maximum gain segment	HM-pattern = 31100: G_{nl} = 1	–	2.28	–	
NON-LINEARITY SETTING AMPNLA (PIN 3); note 3						
$V_{nl(l)}$	control voltage lower limit		–	1.75	–	V
$V_{nl(h)}$	control voltage upper limit		–	3.25	–	V
$I_{ib(nl)}$	input bias current		–	–	0.1	µA
DYNAMICS						
$t_{d(nl)}$	delay between linear and non-linear path		–	–	20	ns
Variable gamma						
VARIABLE GAMMA CONTROL RANGE						
$G_{VAR(min)}$	minimum variable gamma setting		–	0.5	–	
$G_{VAR(max)}$	maximum variable gamma setting		–	1.5	–	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VARIABLE GAMMA SETTING VARGAM (PIN 2); note 3						
$V_{VAR(l)}$	control voltage lower limit		–	1.75	–	V
$V_{VAR(h)}$	control voltage upper limit		–	3.25	–	V
$V_{VAR(lt)}$	control voltage for linear transfer		–	2.5	–	V
I_{ibVAR}	input bias current		–	–	0.1	µA
Colour difference processing						
COLOUR DIFFERENCE INPUTS UIN AND VIN (PINS 5 AND 7)						
$V_{i(UIN)}$	input voltage		1.8	–	–	V
$V_{i(VIN)}$	input voltage		1.8	–	–	V
I_{ib}	input bias current (pins 5 and 7)		–	–	0.1	µA
$V_{i(cl)}$	input voltage level during clamping		–	1.5	–	V
COLOUR DIFFERENCE OUTPUTS (PINS 28 AND 26)						
ΔV_{o28}	output voltage range with respect to the input (pin 28)		150	–	–	%
ΔV_{o26}	output voltage range with respect to the input (pin 26)		150	–	–	%
$V_{o(cl)}$	output voltage level during clamping		–	2.3	–	V
E_{off}	offset error	transparent	–	–	1	%
E_G	gain error	transparent	–	–	5	%
B	bandwidth	transparent	20	30	–	MHz
Timing						
HORIZONTAL WINDOW GENERATION						
fh	line frequency		15	–	16	kHz
Default window setting (with respect to start BK/CLP pulse)						
$t_{dh(ws)}$	default start window		–	$^{6.5}/_{64fh}$	–	
$t_{dhd(wp)}$	default window stop		–	$^{54.5}/_{64fh}$	–	
User window generation with I²C-bus (with respect to start BK/CLP pulse)						
$t_{hws(min)}$	minimum start window		–	$^{4.5}/_{64fh}$	–	
$t_{hws(max)}$	maximum start window		–	$^{19.5}/_{64fh}$	–	
$t_{hwp(min)}$	minimum window stop		–	$^{26.5}/_{64fh}$	–	
$t_{hwp(max)}$	maximum window stop		–	$^{56.5}/_{64fh}$	–	
VERTICAL WINDOW GENERATION						
fv	vertical frequency		45	–	65	Hz
Default window setting (start event with respect to start detected field blanking, stop event with respect to start event)						
t_{dvws}	default window start		–	64	–	lines
t_{dvdwp}	default window stop		–	161	–	lines

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
User window generation with I²C-bus						
$t_{vsw(min)}$	minimum window start		–	10	–	lines
$t_{vsw(max)}$	maximum window start		–	100	–	lines
$t_{vwp(min)}$	minimum window stop		–	121	–	lines
$t_{vwp(max)}$	maximum window stop		–	271	–	lines
Default window select DWS; (pin 1): note 2						
$V_{isc(DWS)}$	voltage input level for window by SC blanking		–	–	1.5	V
$V_{id(DWS)}$	voltage input level for default window		3.5	–	5.5	V
I_{ibDWS}	input bias current	$V_{DWS} = V_{DDA}$	–	–	10	µA
Sandcastle input SC; (pin 10)						
$V_{i(SC)}$	voltage input level	no blanking; no clamp	–	0	1.0	V
		with blanking; no clamp	1.2	1.5	1.8	V
		with blanking and clamp	3.1	3.5	3.9	V
$t_{i(sw)}$	input sync width	no vertical sync	–	–	15	µs
		with vertical sync	35	–	–	µs
CLP PULSE WIDTH RESTORATION						
$t_{d(clp)}$	internal CLP pulse width difference		–	–100	–	ns
I²C-bus specification						
ADDRESS SELECT ADR (PIN 32)						
V_{iADR}	input voltage level	A0 = 0	–	–	1.5	V
		A1 = 1	3.5	–	5.5	V
I_{ibADR}	input bias current		–	–	0.1	µA
TEST PINS TM AND DT (PINS 29 AND 27)						
$V_{i(test)}$	input voltage level		–	–	0.5	V
Overall output performance						
$t_{d(YUV)}$	delay from input to output of YUV	transparent	–	50	100	ns
$t_{dm(YUV)}$	delay of matching YUV	transparent	–	10	20	ns
$\alpha_{w(YUV)}$	crosstalk from window	any channel	–	–	–60	dB

Notes

1. Input amplitude values greater than the minimum specified range are still processed. However, the gain will slowly saturate. Amplitudes up to +4 dB are permitted without significant clipping.
2. This select is valid provided the sleep mode bit is not set.
3. This control is valid provided the sleep mode bit is not set.

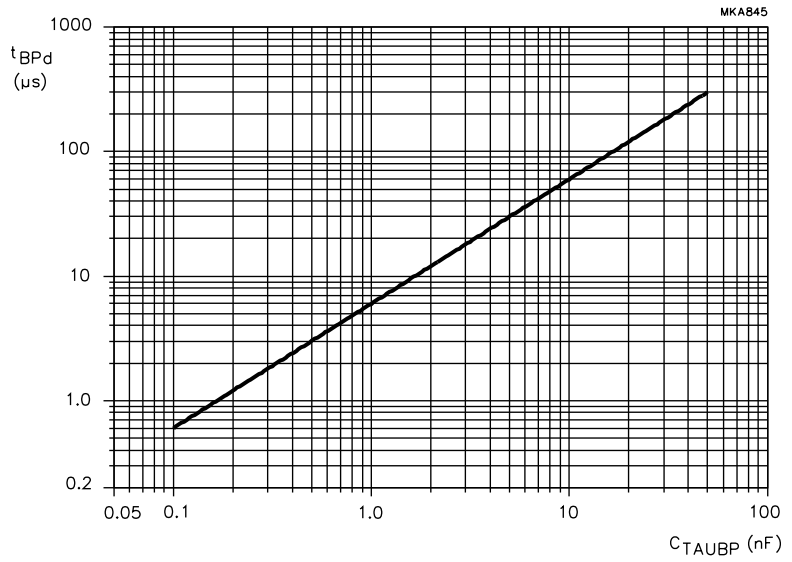
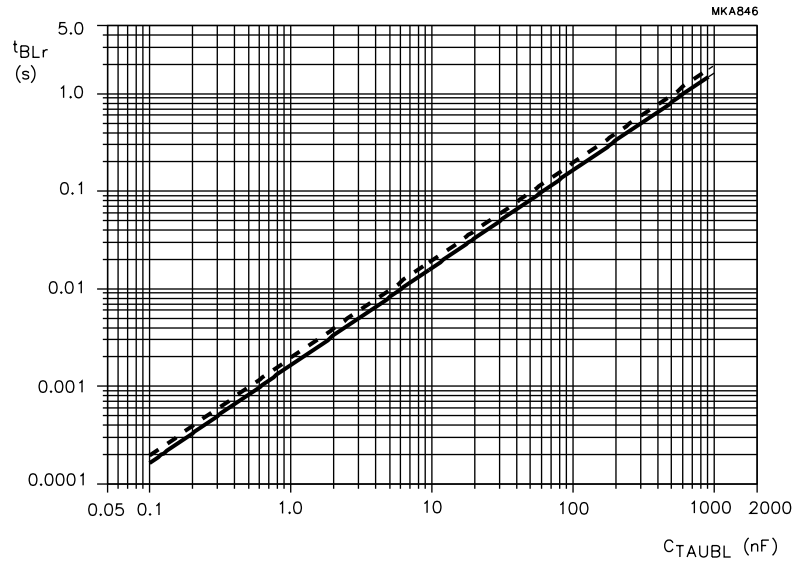
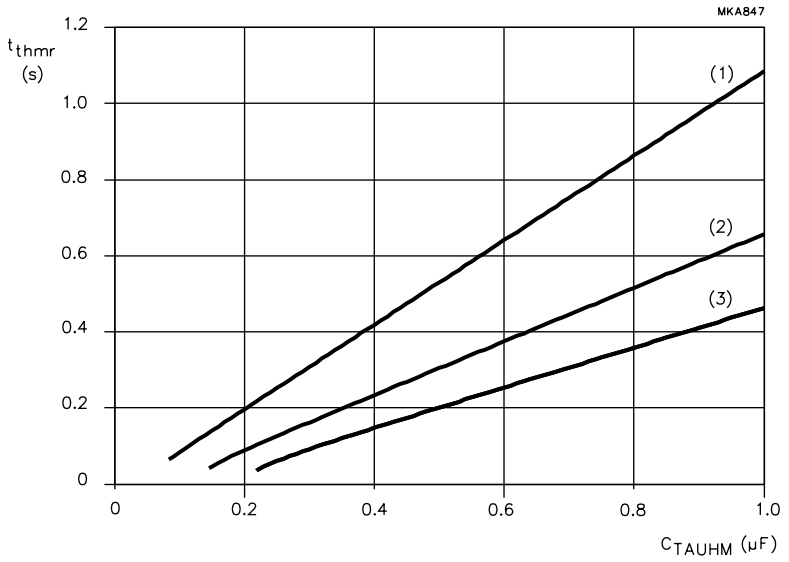


Fig.3 Black occurrence detection time constant as a function of C_{TAUBP}.



The dashed line = 625 lines/frame.
The full line = 525 lines/frame.

Fig.4 Response time constant black level loop as a function of C_{TAUBL}.



(1) Minimum user window.
(2) Default window.
(3) Maximum user window, window by sandcastle blanking.

R_{mc} = 1.

$W_{eff} = t_{hw} \times N_{vw} \times R_{mc}$.

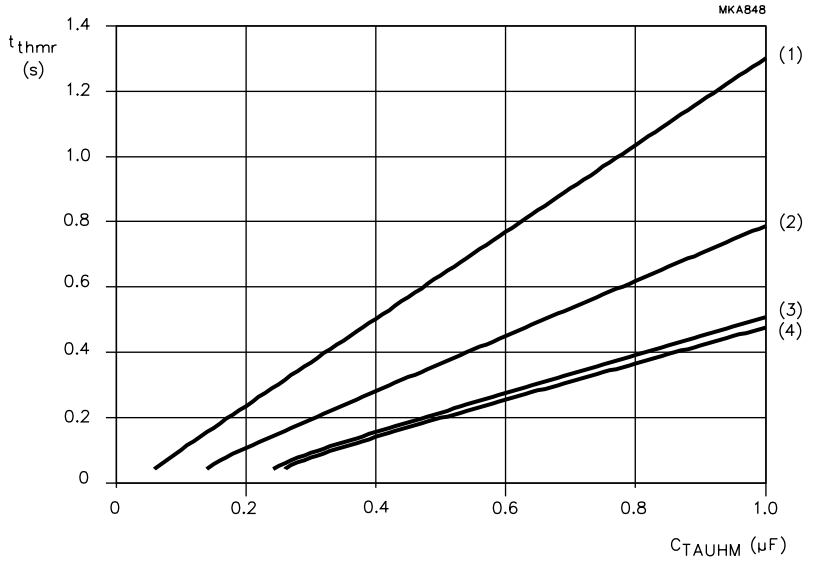
Where:

t_{hw} = horizontal window width (µs).

N_{vw} = vertical window height (lines).

R_{mc} = effective histogram measuring time within window due to miscount in percentage of $t_{hw} \times N_{vw}$.

Fig.5 Response speed of average histogram amplitude control loop as a function of C_{TAUHM} at 60 Hz field-rate.



(1) Minimum user window.
(2) Default window.
(3) Maximum user window.
(4) window by sandcastle blanking.

$R_{mc} = 1$.

$W_{eff} = t_{hw} \times N_{vw} \times R_{mc}$.

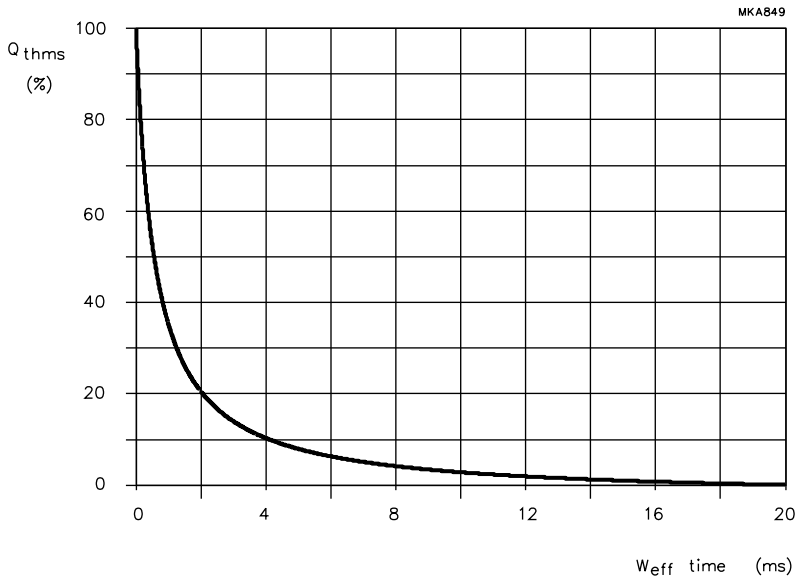
Where:

t_{hw} = horizontal window width (µs).

N_{vw} = vertical window height (lines).

R_{mc} = effective histogram measuring time within window due to miscount in percentage of $t_{hw} \times N_{vw}$.

Fig.6 Response speed of average histogram amplitude control loop as a function of C_{TAUHM} at 50 Hz field-rate.



$W_{eff} = t_{hw} \times N_{vw} \times R_{mc}$.

Where:

t_{hw} = horizontal window width (µs).

N_{vw} = vertical window height (lines).

R_{mc} = effective histogram measuring time within window due to miscount in percentage of $t_{hw} \times N_{vw}$.

Fig.7 Static error on average histogram amplitude (pin TAUHM) as a function of effective histogram measuring time in a field.

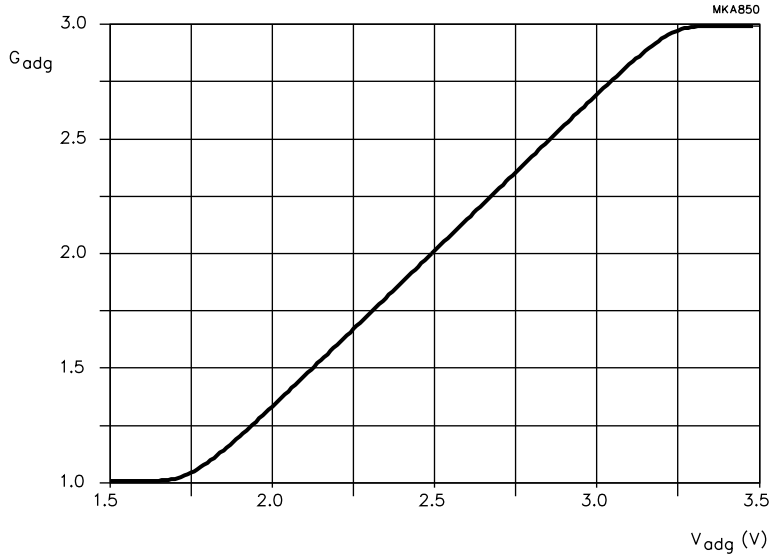


Fig.8 Adaptive gamma gain setting as a function of ADGAM setting in sleep mode.

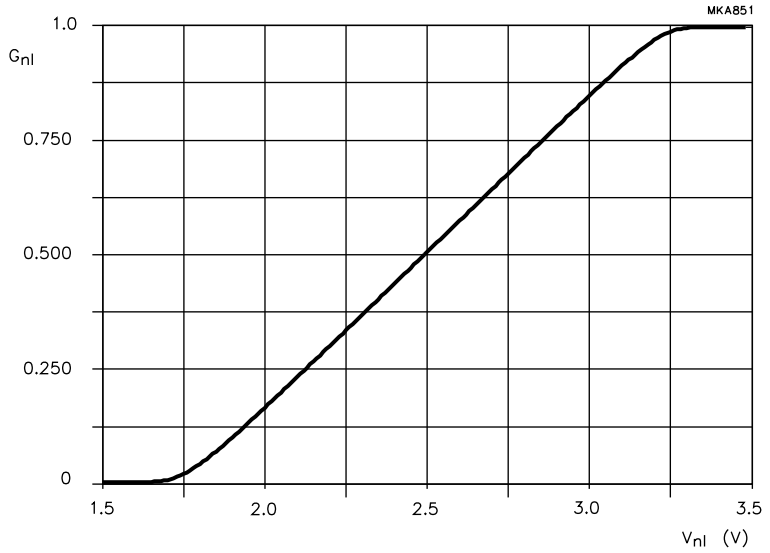


Fig.9 Non-linear amplifier non-linearity setting as a function of AMPNLA setting in sleep mode.

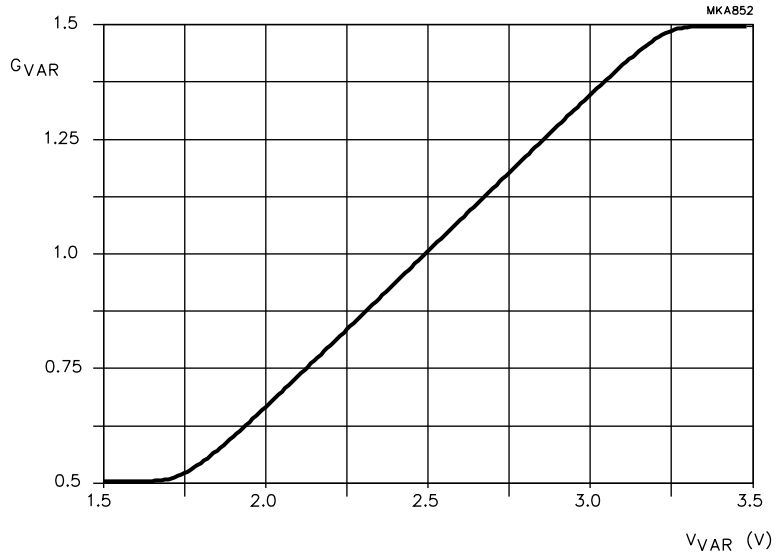


Fig.10 Variable gamma setting as a function of VARGAM setting in sleep mode.

APPLICATION INFORMATION (BUS-MODE)

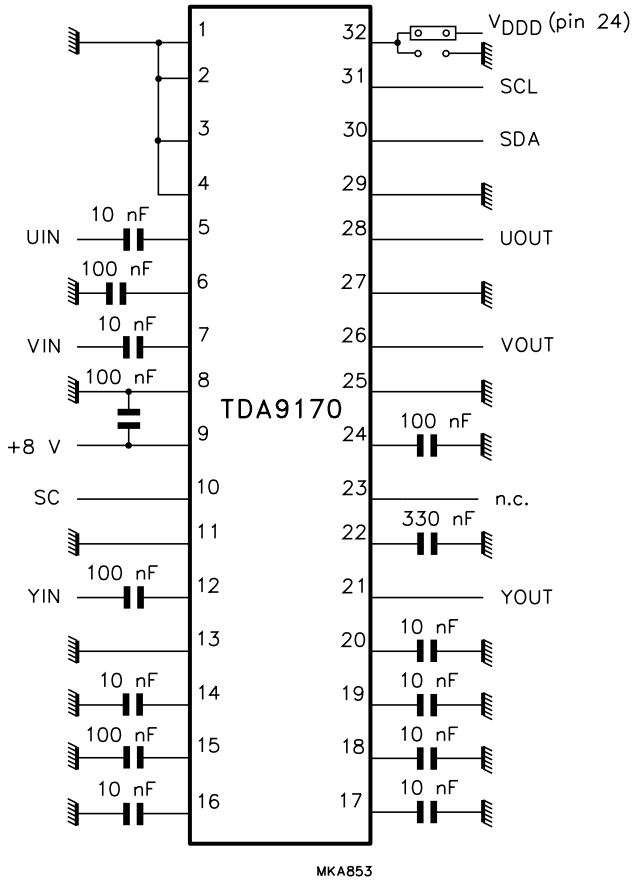


Fig.11 Application diagram.

PACKAGE OUTLINE

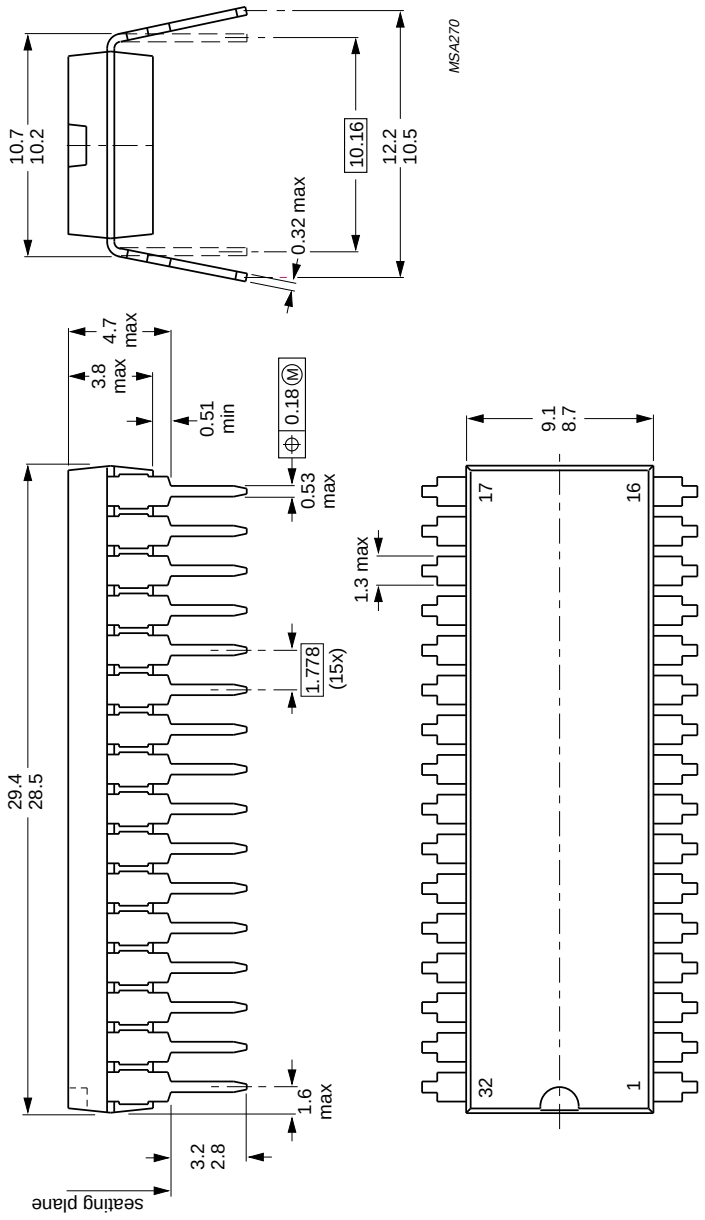


Fig.12 Plastic shrink dual in-line package; 32 leads (400 mil) SDIP32; SOT232-1.

Dimensions in mm.

SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum.

If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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